NOMINAL PERFORMANCE SPECIFICATIONS

TRANSMITTER

Input Data Format: Serial, asynchronous, standard TTL levels

Modulation Technique:
Binary, phase-coherent Frequency Shift Keying (FSK)

TC Output Level: −3 dBm into 600 Ohms

Frequency Accuracy:
+/−0.4 Hz all modems except Bell 202 (MARK)
+1.0 Hz Bell 202 (MARK)

Harmonics: −45 dB from fundamental for single tones

Delay uncertainty for TD logic input change to TC frequency change: ≤ 8.3 μs

Out-of-band energy: See figure 13

RECEIVER

Output Data Format: Serial, asynchronous, TTL level

Demodulation Technique: Differential FM Detection

Sensitivity at Receiver Input: 0 dBm to −48 dBm

Frequency Deviation Tolerance: +/− 16 Hz

Carrier Detect Threshold:
ON >−42dBm +/−1dB
OFF <−48dBm +/−1dB

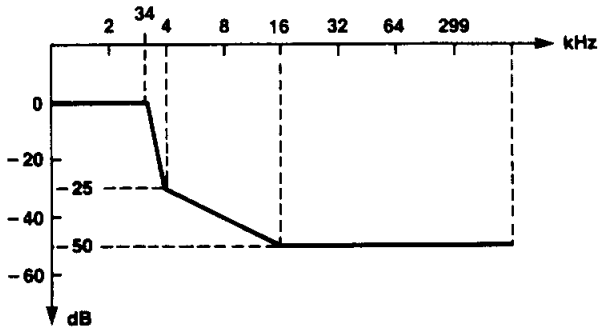

Figure 13. Out-of-band Transmitter Energy

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias . . . . . −10°C to +80°C
Storage Temperature . . . . . −65°C to +150°C
All Input and Output Voltages
with Respect to V_{BB} . . . . . −0.3V to 13V
All Input and Output Voltages
with Respect to V_{CC} . . . . . −13V to 0.3V
Power Dissipation . . . . . 1.0 Watt

D.C. CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5V ± 5%; V_{BB} = −5V ± 5%; AGND = 0V ± 50 mV; DGND = 0V) Typical values are for T_A = 25°C and nominal power supply values.

DIGITAL INTERFACE

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{OH}	Output HIGH Voltage	2.4			VOLTS	I_{OH} = −50 μA, C_{LD} = 50 pF
V_{OL}	Output LOW Voltage			0.4	VOLTS	I_{OL} = +2 mA, C_{LD} = 50 pF
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	VOLTS	
V_{IL}	Input LOW Voltage	−0.5		0.8	VOLTS	
V_{IHC}	External Clock Input HIGH	3.8		V_{CC}	VOLTS	
V_{ILC}	External Clock Input LOW	−0.5		0.8	VOLTS	
V_{IHR}	External Reset Input HIGH	3.8		V_{CC}	VOLTS	
V_{ILR}	External Reset Input LOW	−0.5		0.8	VOLTS	
I_{IL}	Digital Input Leakage Current	−10		+10	μA	$0 \leq V_{IN} \leq V_{CC}$
C_{OUT}	Output Capacitance		5	15	pF	f_C = 1.0 MHz
C_{IN}	Input Capacitance		5	15	pF	f_C = 1.0 MHz

ANALOG

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
R_{IN}	Input Resistance	50			KOHMS	$-1.6\ V < V_{RC} < +1.6V$
V_{RC}	Operating Input Signal	−1.6		+1.6	V	
V_{RCOS}	Allowed DC Input Offset	−30		+30	mV	REF VAGND
V_{TC}	Output Voltage	−1.1		+1.1	V	R_L = 600 Ω
V_{TCOS}	Output DC Offset		±200		mV	

POWER DISSIPATION

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
I_{CC}	V_{CC} Supply Current			125	mA	
I_{BB}	V_{BB} Supply Current			25	mA	

Table 5. Handshake Initial Conditions*

Data Terminal Ready ($\overline{DTR}$)	OFF
Request to Send ($\overline{RTS}$)	OFF
Clear to Send ($\overline{CTS}$)	OFF
Transmitted Data (TD)	Ignored
Back Channel Request to Send ($\overline{BRTS}$)	OFF
Back Channel Clear to Send ($\overline{BCTS}$)	OFF
Back Channel Transmitted Data (BTD)	Ignored
Ring ($\overline{RING}$)	OFF
Carrier Detect ($\overline{CD}$)	OFF
Received Data (RD)	MARK
Back Channel Carrier Detect ($\overline{BCD}$)	OFF
Back Channel Received Data (BRD)	MARK

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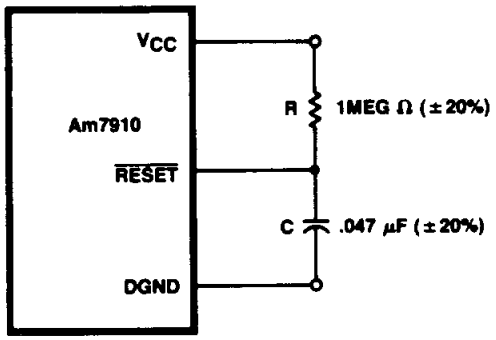
POWER ON RESET

The reset circuit operates in either of two modes.

Automatic Reset

In this mode an internal reset sequence is automatically entered when power is applied to the device. One resistor and one capacitor must be connected externally as shown in Figure 11. Values shown will work with most power supplies. Power supply (V_{CC}) rise time should be less than one half the RC time constant.

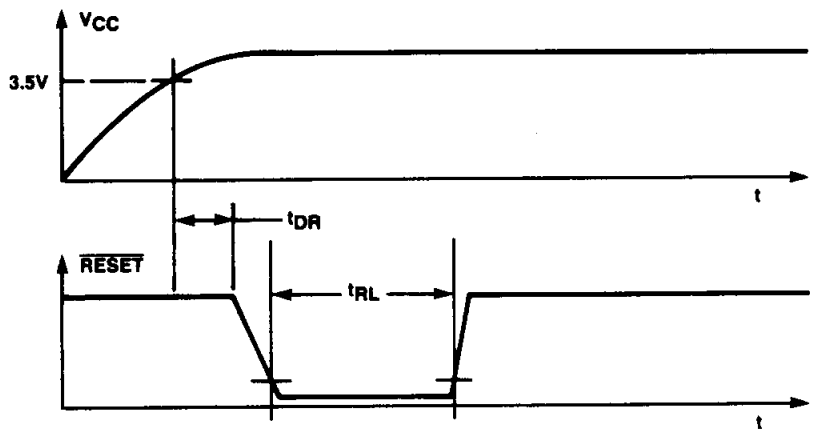
Figure 11. Automatic Reset*



External Reset

In this mode the device may be forced into the reset sequence by application of an active LOW pulse applied to the $\overline{RESET}$ input. The reset must not be applied until the V_{CC} supply has reached at least 3.5 V. Timing is diagrammed in Figure 12.

Figure 12. External Reset*
TIMING DIAGRAMS



t_{DR} = delay from the time V_{CC} reaches 3.5 V and the falling edge of $\overline{RESET}$ signal (>1 μs)

t_{RL} = $\overline{RESET}$ LOW duration time (>t_{MCK} = 406 ns)

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CLOCK GENERATION

Master timing of the modem is provided by either a crystal connected to the $XTAL_1$ and $XTAL_2$ inputs or an external clock applied to the $XTAL_1$ input.

Crystal

When a crystal is used it should be connected as shown in Figure 13. The crystal should be a parallel resonance type, and its value must be 2.4576 MHz ± .01%. A list of crystal suppliers is shown below.

External Clock

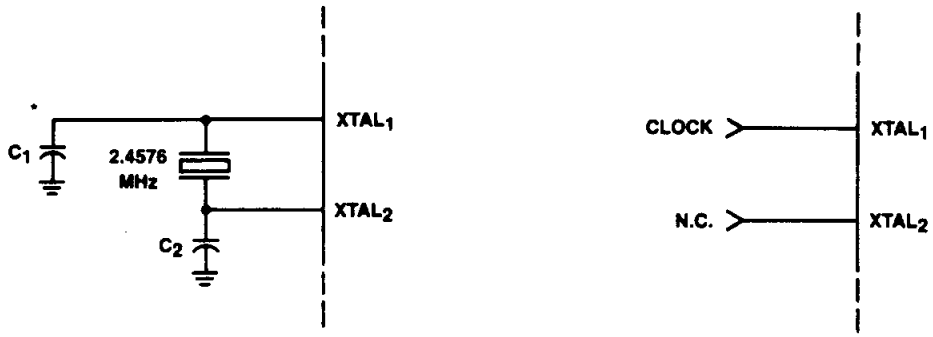
This clock signal could be derived from one of several crystal-driven baud rate generators. It should be connected to the $XTAL_1$ input and the $XTAL_2$ input must be left floating. The timing parameters required of this clock are shown in Figure 10 and the values are listed in Table 4.

Figure 10. Clock Generation*

Crystal Information (f_C = 2.4576 MHz)

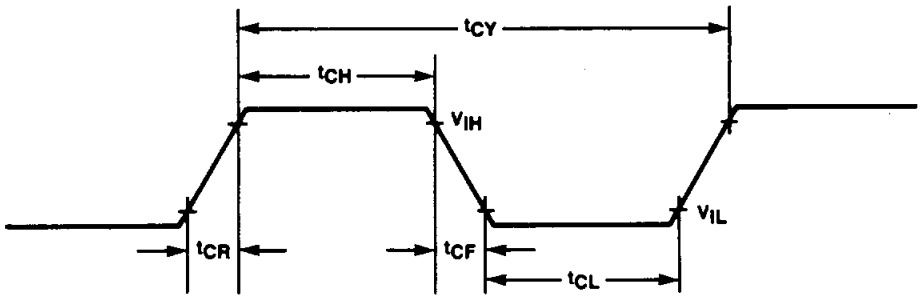
Manufacturer	P/N	C_1	C_2
M-Tron	MP-2	20 pF	20 pF
Monitor Products	MM-33	20 pF	20 pF

Note: Rise time of V_{CC} must be greater than 5 msec to insure proper crystal oscillator start-up.



*Capacitors values vary with different crystal manufacturers.

(a)



(b)

Table 4. Clock Parameters*

Symbol	Parameters	Min	Typ	Max	Units
t_{CY}	Clock Period	406.86	406.9	406.94	ns
t_{CH}	Clock High Time	165			ns
t_{CL}	Clock Low Time	165			ns
t_{CR}	Clock Rise Time			20	ns
t_{CF}	Clock Fall Time			20	ns

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Figure 9. BELL 103/CCITT V.21 Handshake Timing*

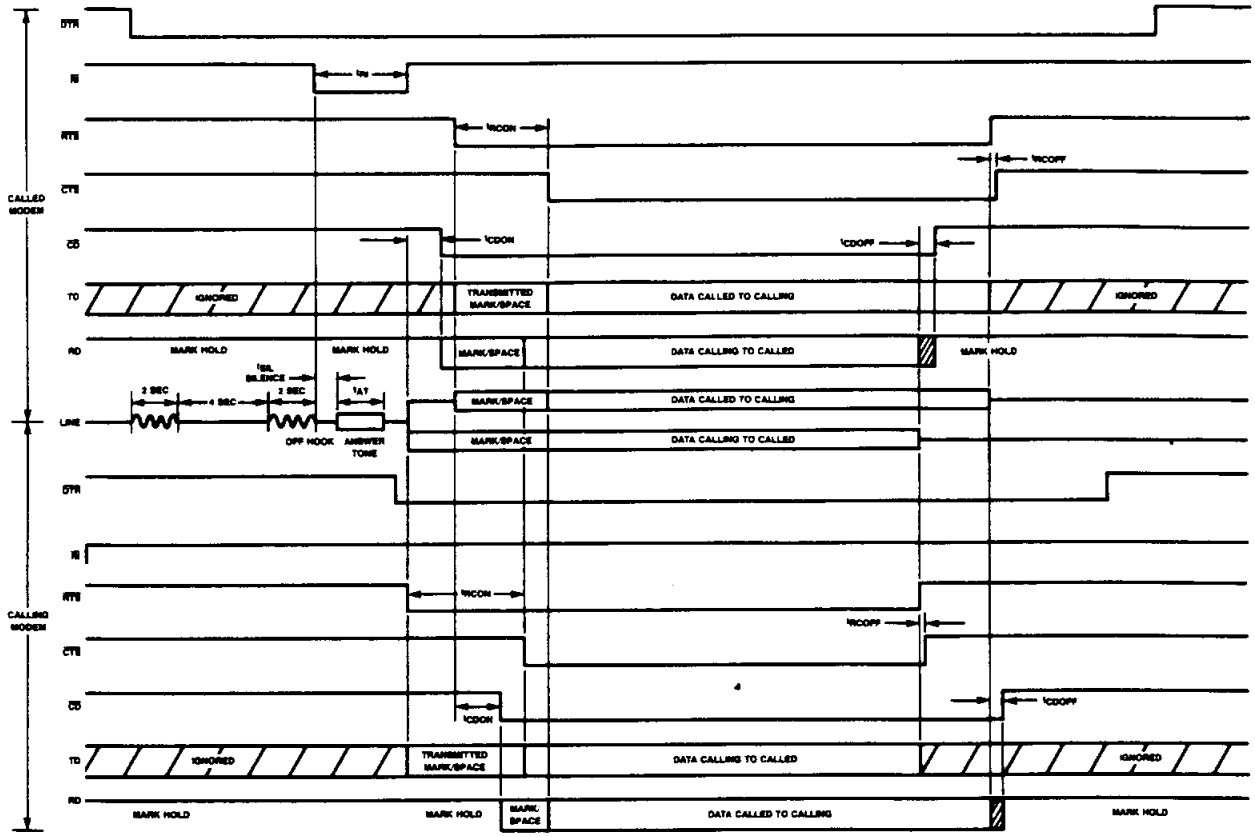

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Figure 8. CCITT V.23 Handshake Timing*

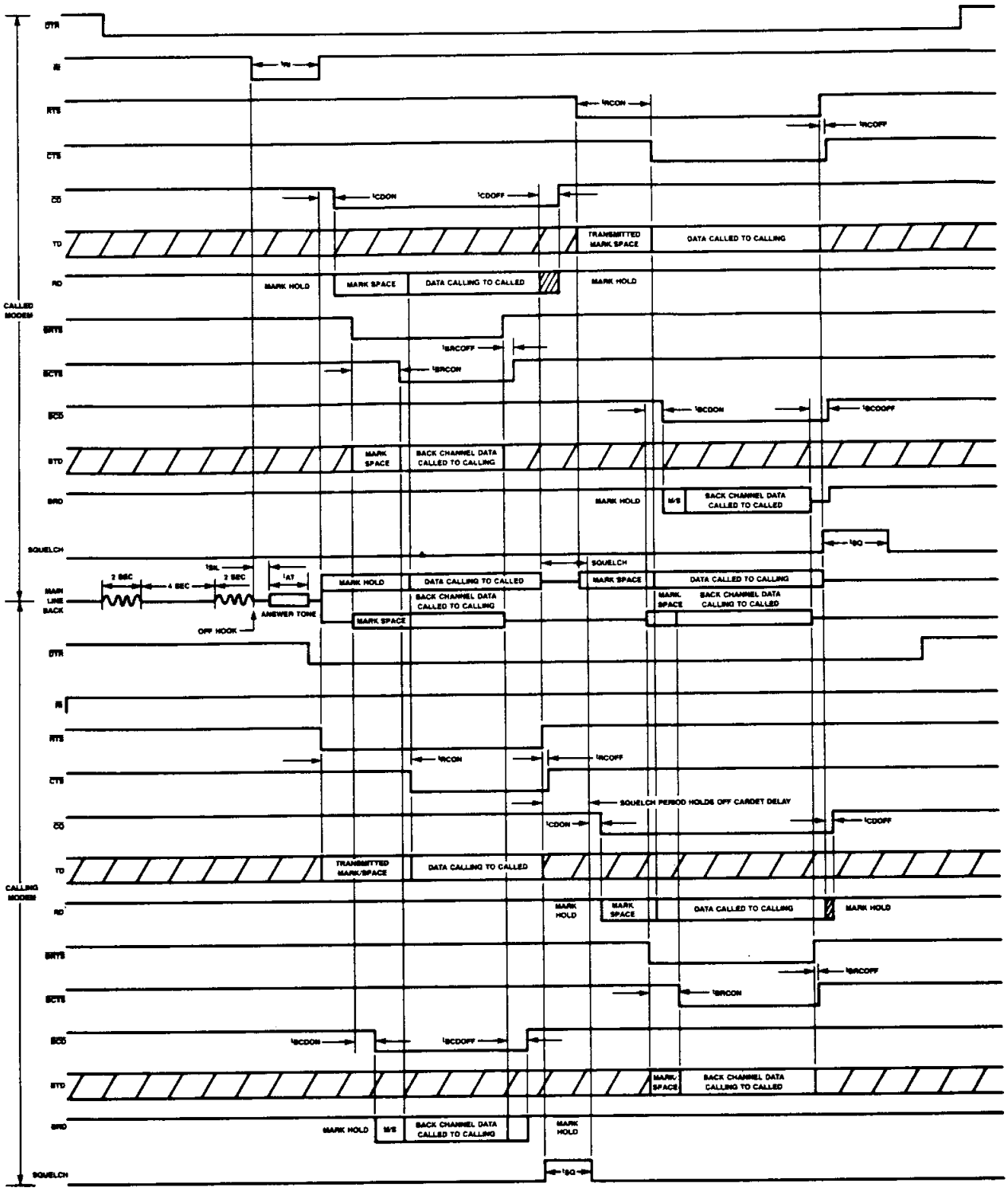

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Figure 7. BELL 202 Handshake Timing*

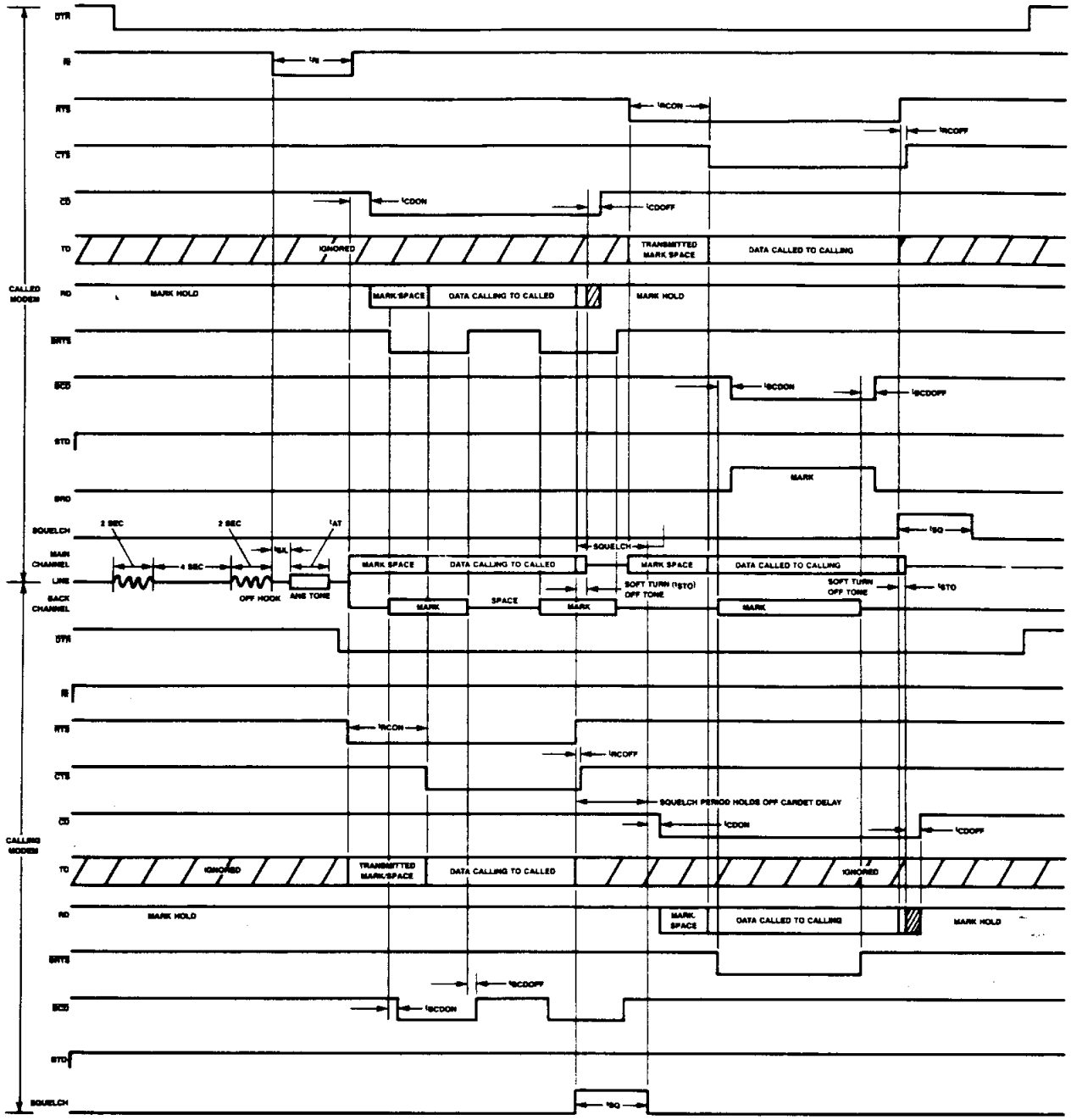

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Figure 6. Receiver Main/Back Channel State Diagram*

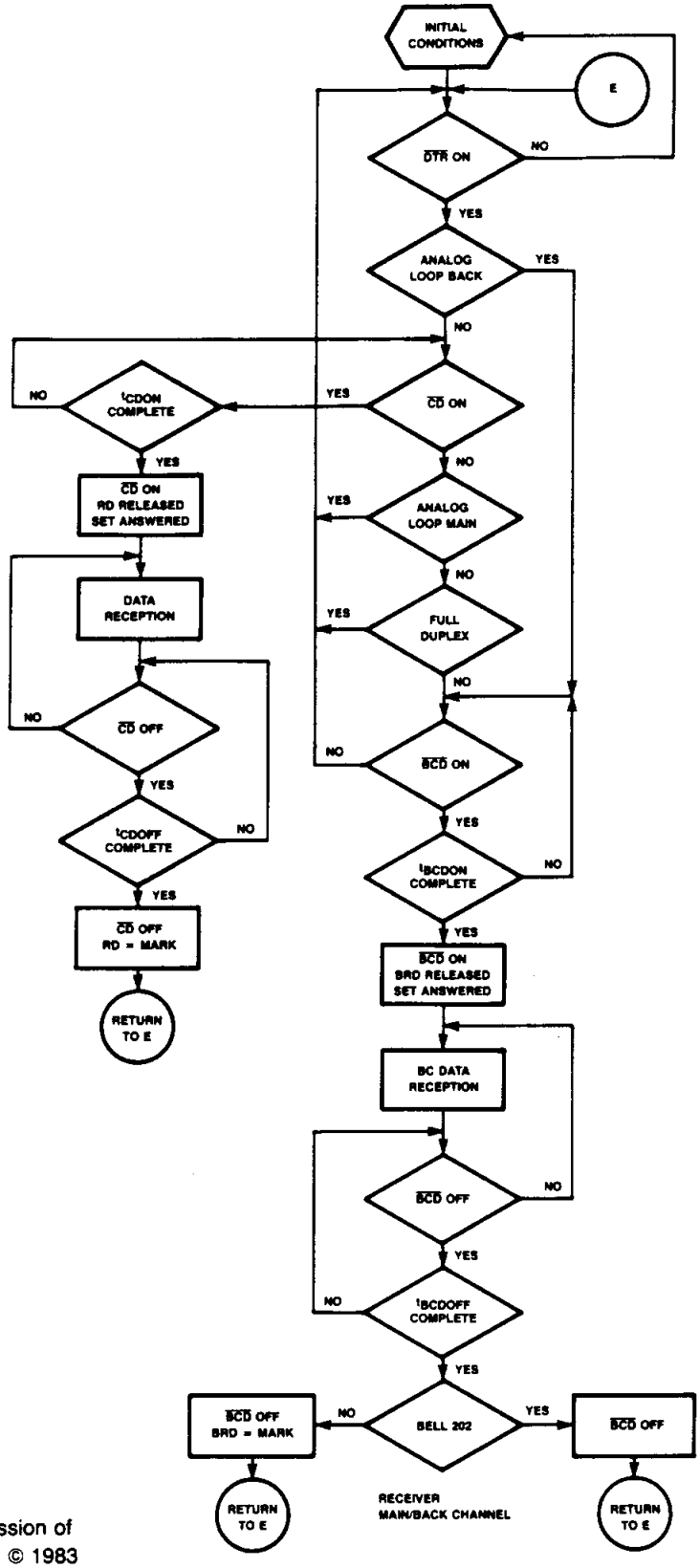

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Figure 5(b). Transmit Back Channel State Diagram*

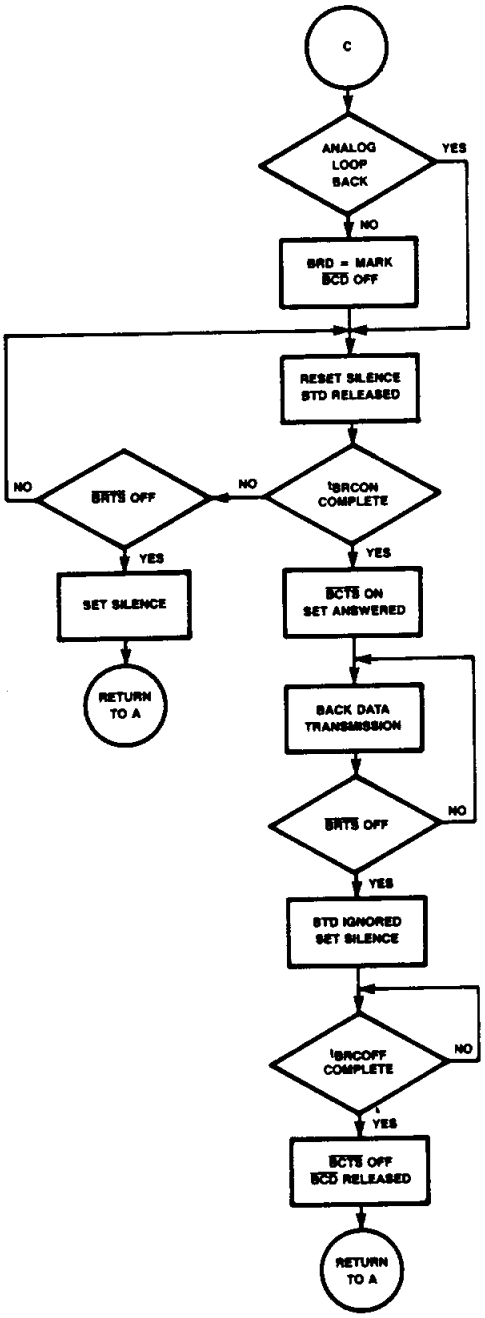


Figure 5(c). Auto Answer State Diagram*

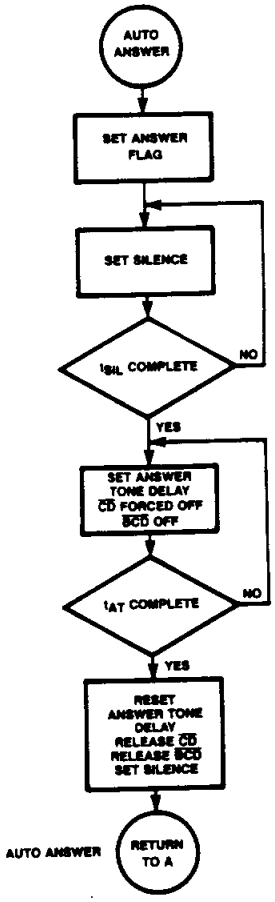
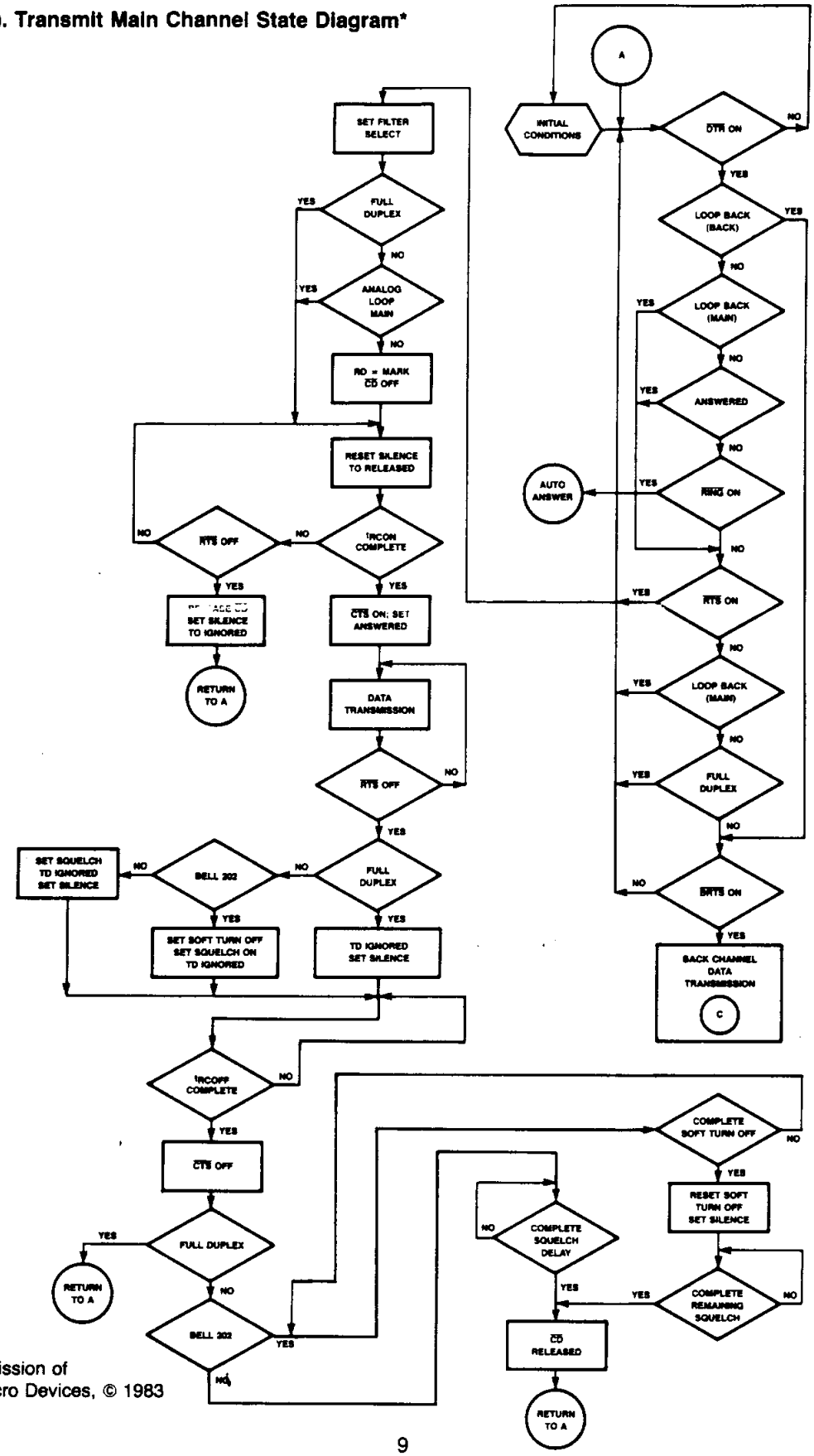


Figure 5(a). Transmit Main Channel State Diagram*



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GENERAL OPERATION

Functional Blocks

As is shown in Figure 2, the i2970 consists of three functional sections; Transmit Channel, Receive Channel, and Control.

The Transmit Channel consists of a sine synthesizer and bandpass filters, implemented digitally (through Digital Signal Processing (DSP) techniques), a Digital to Analog Converter (DAC), and an analog post filter. Binary data is presented to the 2970's transmitter at TD. The sine synthesizer, under mode control, performs the FSK modulation of the binary data (in digital format).

Modulation by FSK is a technique whereby two states of a binary signal, are represented by two frequencies of a carrier. As the incoming (TD) binary signal causes the carrier frequency to shift from one frequency to the other, undesirable frequencies are produced. These undesirable frequencies are effectively rejected by the DSP bandpass filters.

The modulated carries is then passed to the DAC where it is converted to analog. The analog post filter smooths the carrier before transferring the modulated analog signal on TC, to a DAA, or acoustic coupler for phone line transmission.

The Receive Channel comprises an analog prefilter, an Analog to Digital Converter (ADC), and bandpass filters, demodulator, and carrier detect stages also implemented through DSP technology. The modulated data is presented to the 2970's receiver at RC, from the DAA or acoustic coupler. The analog prefilter performs the anti-alias conditioning required by the sampling process that follows. The modulated carrier is then sampled by the ADC before being passed to the digital bandpass filters. The conditioned signal is demodulated to recover the binary information. Additionally, the output of the digital bandpass filter stage is also routed to a carrier detector that outputs a carrier detect signal to indicate the presence of a carrier.

The Interface/Control block performs the handshaking between the i2970 and the local Data Terminal Equipment (DTE) and configures the transmit and receive channels for the appropriate transmission rates. For interface control, the i2970 features RS232C/V.24 handshaking for both main and back channels; Request to Send, Clear to Send, and Data Terminal Ready. For 300 bps FDX modes, the back channel signals are non-functional.

For internal modem control the filters and transmission/reception rates are configured by two state machines through the mode control pins, MC0–4. The $\overline{\text{RING}}$ input and Carrier Detect output are used for call establishment and automatic answering capability. Figures 5 and 6 present flowcharts of the two state machines for call set-up Figures 7, 8, and 9 specify the handshake timing sequencing. Table 5 indicates the initial state of the handshaking pins.

CALL ESTABLISHMENT

Handshaking for call establishment not only occurs between the modem and the DTE, but must also occur between the originate and answer modems on the line. This handshaking can occur either manually or automatically.

In manual call set-up, the user dials the number and upon receipt of an answer, would place the modem in data transmission mode, and the two modems would be free to begin transmission.

In automatic call set-up, the call originating modem, through the use of a Automatic Calling Unit (ACU) would generate the dial pulse or tones needed to contact the answering modem. The answering modem would sense the ringing sequence through the DAA, take the phone 'off-hook', and then initiate a call answering sequence. The call-answering sequence consists of silent duration followed by an answer tone. The ACU of the originating modem has the ability to detect the answer tone and then place the modem into data transmission mode. The two modems are now free to communicate.

The i2970 has the capability of providing the automatic answering sequence. This can be accomplished by applying the ring signal from the DAA to the i2970's $\overline{\text{RING}}$ input. Upon detection of a TTL low at the $\overline{\text{RING}}$ input, the i2970 begins the auto-answer sequence (assuming that DTE to modem configuration is already established).

The sequence begins with a silent interval output on TC for a time, t_{SIL}, followed by an answer tone of duration, t_{AT}. During this time the Carrier Detect pin is brought high (OFF), and the Receive Data output is also held high (MARK). Upon completion of the sequence, $\overline{\text{CD}}$ is released. If the modem is configured for V.23 or 202 modes, the transmit filters are set for the main channel while the receive filters are set for back channel. During the auto-answer sequence, an answer flag is set within the state machine process. If the auto-answer sequence needs to be entered again, the answer flag must be reset and this is accomplished by turning $\overline{\text{DTR}}$ first OFF, then ON, again. Tying $\overline{\text{RING}}$ high will disable auto-answering for manual applications. Review of the flowchart presented in Table 8 describes the auto-answer sequence in detail.

Table 3(b). Timing Parameters (Refer to Figures 8, 9 and 10 for Timing Diagrams)*

Symbol	Description	Bell 103 Orig	Bell 103 Ans	CCITT V.21 Orig	CCITT V.21 Ans	CCITT V.23 Mode 1	CCITT V.23 Mode 2	CCITT V.23 Mode 2 EQ	Bell 202	Bell 202 EQ	CCITT V.23 Back	Bell 202 Back	Unit
$t_{RC(On)}$	Request-to-Send to Clear-to-Send ON Delay	208.3	208.3	400	400	208.3	208.3	208.3	183.3	183.3	—	—	msec ±0.3%
$t_{RC(off)}$	Request-to-Send to Clear-to-Send OFF Delay	0.3–0.5	0.3–0.5	0.3–0.5	0.3–0.5	0.3–0.5	0.3–0.5	0.3–0.5	0.3–0.5	0.3–0.5	—	—	msec ±0.25%
$t_{BRC(On)}$	Back Channel Request-to-Send to Clear-to-Send ON Delay	—	—	—	—	—	—	—	—	—	82.3	—	msec ±0.64%
$t_{BRC(Off)}$	Back Channel Request-to-Send to Clear-to-Send OFF Delay	—	—	—	—	—	—	—	—	—	0.5	—	msec ±25%
$t_{CD(On)}$	Carrier Detect ON Delay	93–106	93–106	301–312	301–312	11.4–15.4	11.4–15.4	11.4–15.4	18–22	18–22	—	—	msec
$t_{CD(Off)}$	Carrier Detect OFF Delay	21–40	21–40	21–40	21–40	5.4–13.3	5.4–13.3	5.4–13.3	12.4–23.4	12.4–23.4			msec
$t_{BCD(On)}$	Back Channel Carrier Detect ON Delay	—	—	—	—	—	—	—	—	—	17–25	17–25	msec
$t_{BCD(Off)}$	Back Channel Carrier Detect OFF Delay	—	—	—	—	—	—	—	—	—	21–38	21–38	msec
t_{AT}	Answer Tone Duration	—	1.9	—	3.0	3.0	3.0	3.0	1.9	1.9	—	—	sec ±0.44%
t_{SIL}	Silence Interval before Transmission	1.3	1.3	1.9	1.9	1.9	1.9	1.9	1.3	1.3	—	—	sec ±0.64%
t_{SQ}	Receiver Squelch Duration	—	—	—	—	156.3	156.3	156.3	156.3	156.3	—	—	msec ±3.3%
t_{STO}	Transmitter Soft Turn-Off Duration	—	—	—	—	—	—	—	24	24	—	—	msec ±2.3%
t_{RI}	Minimum $\overline{RI}$ Low Duration	—	25	—	25	25	25	25	25	25	—	—	μs

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Figure 4. Half Duplex*

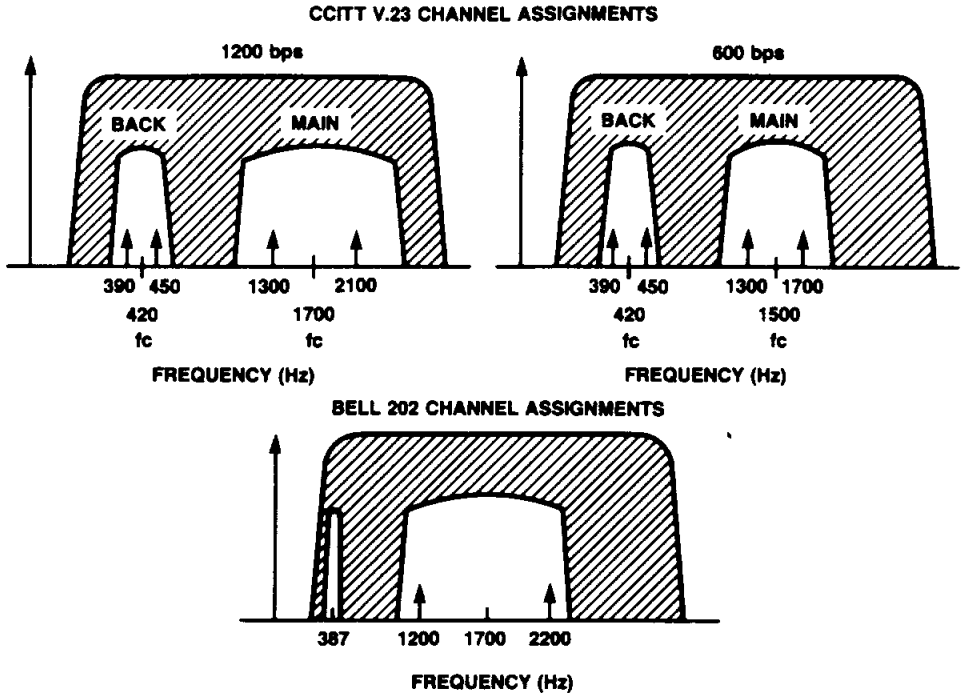

Table 3(a). Frequency Parameters*

Modem	Baud Rate (BPS)	Duplex	Transmit Frequency		Receive Frequency		Answer Tone Freq Hz
			Space Hz	Mark Hz	Space Hz	Mark Hz	
Bell 103 Orig	300	Full	1070	1270	2025	2225	—
Bell 103 Ans	300	Full	2025	2225	1070	1270	2225
CCITT V.21 Orig	300	Full	1180	980	1850	1650	—
CCITT V.21 Ans	300	Full	1850	1650	1180	980	2100
CCITT V.23 Mode 1	600	Half	1700	1300	1700	1300	2100
CCITT V.23 Mode 2	1200	Half	2100	1300	2100	1300	2100
CCITT V.23 Mode 2 Equalized	1200	Half	2100	1300	2100	1300	2100
Bell 202	1200	Half	2200	1200	2200	1200	2025
Bell 202 Equalized	1200	Half	2200	1200	2200	1200	2025
CCITT V.23 Back	75	—	450	390	450	390	—
Bell 202 Back	5	—	*	*	**	**	—

*($\overline{\text{BRTS}}$ LOW) and (BTD HIGH): 387 Hz at TC
*($\overline{\text{BRTS}}$ HIGH) or (BTD LOW): 0 volts at TC
**387 Hz at RC: $\overline{\text{BCD}}$ LOW
**No 387 Hz at RC: $\overline{\text{BCD}}$ HIGH
*Meets new CCITT V.20 frequency tolerance.

Frequency tolerance is less than ±0.4 Hz with 2.4576 MHz Crystal. Except Bell 202 which is +1 Hz (1200 Hz, mark)

Table 2. Mode Control

PINS					Configuration
MC4	MC3	MC2	MC1	MC0	
0	0	0	0	0	Bell 103 Originate, 300 bps Full Duplex
0	0	0	0	1	Bell 103 Answer
0	0	0	1	0	Bell 202, 1200 bps Half Duplex
0	0	0	1	1	Bell 202, W/Equalizer
0	0	1	0	0	CCITT V.21 Originate, 300 bps Full Duplex
0	0	1	0	1	CCITT V.21 Answer
0	0	1	1	0	CCITT V.23 Mode 2, 1200 bps Half Duplex
0	0	1	1	1	CCITT V.23 Mode 2, W/Equalizer
0	1	0	0	0	CCITT V.23 Mode 1, 600 bps Half Duplex
		•		}	Reserved
		•			
		•			
1	0	0	0	0	Bell 103 Originate Loopback
1	0	0	0	1	Bell 103 Answer Loopback
1	0	0	1	0	Bell 202 Main Loopback
1	0	0	1	1	Bell 202 W/Equalizer Loopback
1	0	1	0	0	CCITT V.21 Originate Loopback
1	0	1	0	1	CCITT V.21 Answer Loopback
1	0	1	1	0	CCITT V.23 Mode 2 Main Loopback
1	0	1	1	1	CCITT V.23 Mode 2 W/Equalizer Loopback
1	1	0	0	0	CCITT V.23 Mode 1 Main Loopback
1	1	0	0	1	CCITT V.23 Back Loopback
		•		}	Reserved
		•			
		•			

FUNCTIONAL DESCRIPTION

The i2970 is a Frequency Shift Keyed (FSK) modem. As such, the i2970 modulates low speed, serial, asynchronous data to an analog signal suitable for transmission over the telephone network, in one direction, and demodulates analog to digital format in the other. The i2970 is capable of transmitting and/or receiving data at bit rates of 300 bps full duplex (2-wire), 600 bps half duplex, and 1200 bps half duplex (with additional back channel capability of 75/5 bps for split channel operation) conforming to European (CCITT) and North American (Bell) standards. Figure 3 shows the channel assignments for full duplex operation. Figure 4 shows the channel assignments for half duplex operation.

Figure 3. Full Duplex*

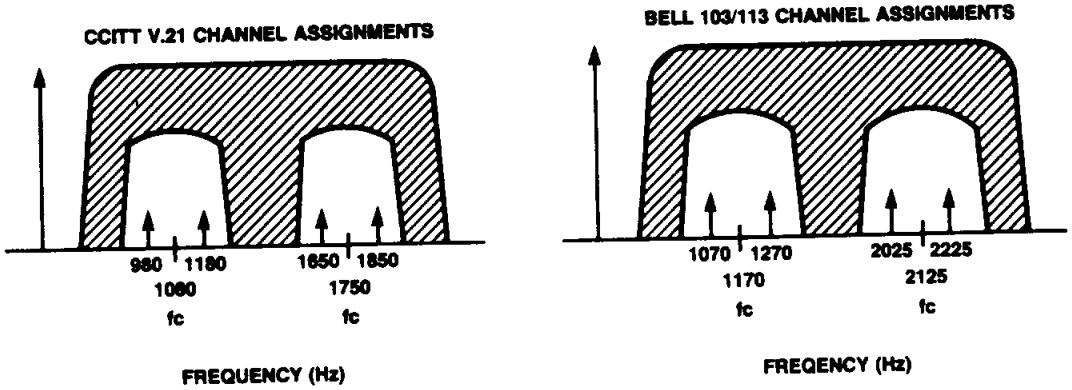

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Table 1. Pin Description (Continued)

Symbol	Function
TC	Transmitted Carrier. Transmit data is modulated and converted to analog for phone line transmission at this output.
RC	Received Carrier. Received analog modulated waveform is presented at this input for de-modulation.
TD	Transmitted Data. Application of logical data serially at this input is modulated by the modem for phone line transmission at TC.
RD	Received Data. Received modulated data is demodulated by the modem and is available in serial logic format at this pin.
BTD	Backchannel Transmitted Data. For Bell 202 or CCITT V.23 this input is used for backchannel data, just as TD for the main channel. For 202 on/off keying, BTD should be held high.
BRD	Backchannel Received Data. For CCITT V.23 this output is used as the backchannel for demodulated data. This output is forced high under the following conditions: 1) BRD high, 2) $\overline{\text{DTR}}$ high, 3) V.21/103 mode, 4) During auto-answer, and 5) When $\overline{\text{BRTS}}$ ON and RTS OFF in V.23 mode only.
$\overline{\text{CD}}$	Carrier Detect. Indicates the recognition of a carrier at the receiver input. If the output is low, a valid carrier signal has been present at the receiver for at least a time tCDON, conversely, if the output is high, a carrier has not been detected at the receiver for at least a time tCDOFF, or $\overline{\text{DTR}}$ is high.
$\overline{\text{BCD}}$	Backchannel Carrier Detect. For CCITT V.23 or Bell 202, this output signifies the detection of the backchannel carrier. For V.23, $\overline{\text{BCD}}$ turns on whenever the MARK or SPACE frequency appears. For 202, $\overline{\text{BCD}}$ turns on in response to a 387 Hz tone.
$\overline{\text{DTR}}$	Data Terminal Ready. Input to the modem to indicate whether the data terminal is prepared to send or receive data. This input is gated with all other i2970 TTL I/O in order to enable/disable all these signals as well as to allow the internal control logic to function.
$\overline{\text{RTS}}$	Request To Send. Modem is alerted through this input to enter the transmit mode. This signal must stay low for the duration of transmitting data.
$\overline{\text{BRTS}}$	Backchannel Request To Send. Equivalent to $\overline{\text{RTS}}$ for the backchannel, in CCITT V.23 or Bell 202 modes.
$\overline{\text{CTS}}$	Clear To Send. After receiving a $\overline{\text{RTS}}$ input, modem alerts DTE through this output that it is prepared to receive transmitted data. Actual data should not be presented to the Transmitted Data input until $\overline{\text{CTS}}$ has gone low. Normally the user should force TD high whenever $\overline{\text{CTS}}$ is off.
$\overline{\text{BCTS}}$	Backchannel Clear To Send. Equivalent to $\overline{\text{CTS}}$ for the backchannel, in CCITT V.23 or Bell 202 modes.
$\overline{\text{RING}}$	Auto-answer ring input from the DAA.
MC0–MC4	Mode Control 0–4. These are the mode control pins used to configure the i2970 to the modem standard desired. Up to 32 different modes can be specified, as shown in Table 2, however, only 19 different configurations are actually available for use.

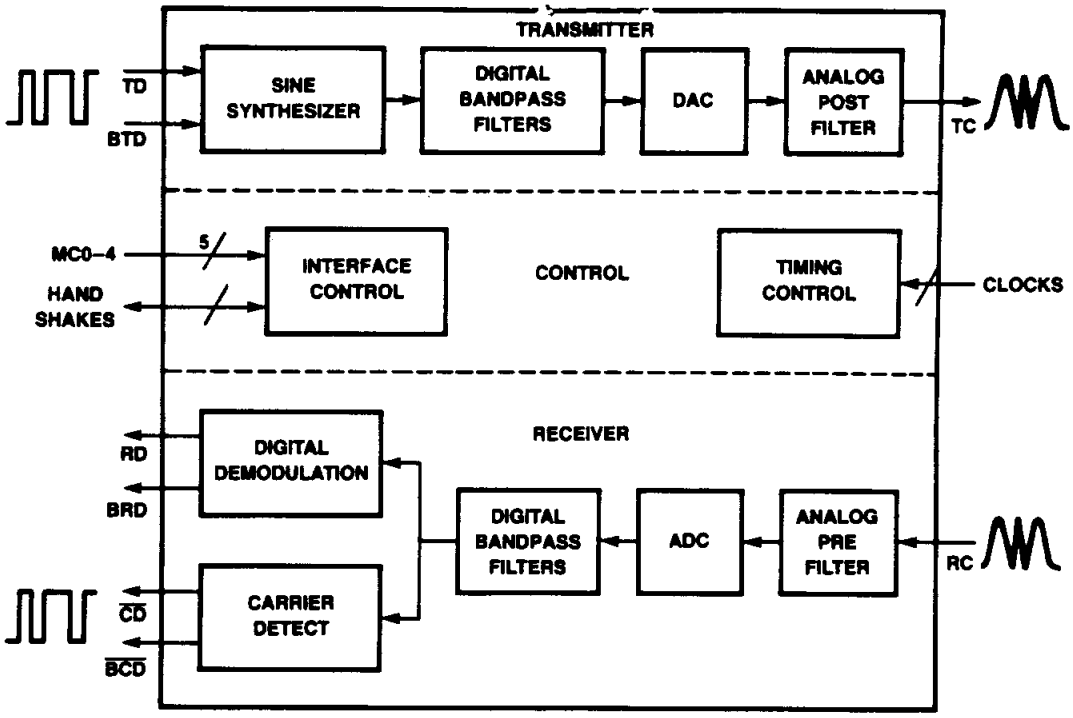

Figure 2. 2970 Block Diagram

Table 1. Pin Description

Symbol	Function
Vcc	Most positive supply; input voltage is +5 ± 5% ref to GNDD.
Vbb	Most negative supply; input voltage is −5 ± 5% ref to GNDD.
GNDA	Analog ground, not internally connected to GNDD.
GNDD	Digital ground, not internally connected to GNDA.
CAP1/CAP2	Capacitor inputs for A/D converter. External capacitor/resistor network required.
XTAL1/XTAL2	Crystal inputs for internal clocking or XTAL1 pin can be used instead with an external clock.
$\overline{\text{RESET}}$	Input to an internal reset circuit. The device is reset by application of an external active low TTL signal.

2970
SINGLE-CHIP FSK MODEM WITH FILTERS

- **300 BPS Full Duplex Exceeds CCITT V.21 Bell 103/113/108 1200 BPS Half Duplex Exceeds CCITT V.23 and Bell 202**
- **5 Pin Mode Control for Modem Configuration**
- **Auto-Answer, Loopbacks Provided**
- **Pin-for-Pin Compatible with AM7910**
- **Complete RS232/V.24 Handshaking**
- **Surpasses Military Electrostatic Discharge Specification (MIL STD 883B Method 3015.1)**

The Intel i®2970 single-chip, 28 pin, FSK modem is pin-for-pin compatible with the AMD 7910. The i2970 is a fully equipped modem with filters realized through highly stable digital signal processing technology. It is fabricated in a proven reliable N-channel HMOS silicon gate technology (HMOS-E). This modem is manufactured on a high volume analog production line using state-of-the-art test equipment, and passes Intel's stringent quality and reliability requirements.

The primary applications for the i2970 are for database access, e.g., Videotex, and Point-of-Sales terminals. Other applications include industrial control/remote monitoring and telemetry. A Data Access Arrangement (DAA) or acoustic coupler must externally provide the phone line interface.

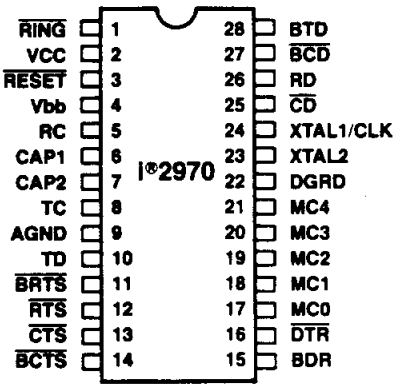

Figure 1. Pin Configuration

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